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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,460	07/03/2003	Phillip Johnson	1054.023	6552

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MENDELSOHN AND ASSOCIATES PC
1515 MARKET STREET
SUITE 715
PHILADELPHIA, PA 19102

EXAMINER	
CHANG, JOSEPH	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/613,460	JOHNSON ET AL.	
	Examiner	Art Unit	
	Joseph Chang	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18-21* is/are allowed.

6)☒ Claim(s) *1-10 and 16* is/are rejected.

7)☒ Claim(s) *11-15 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9, 16, are rejected under 35 U.S.C. 102(b) as being anticipated by Tran US 6373342.

Regarding Claim 1, Tran discloses in Figures 4 and 9 a circuit comprising a set of interconnected delay stages (three inverter circuit 30, Col. 4, lines 29-45); and switched-controlled load circuitry (21, 22, 24) (in-line transistor 24 functions as a switch, Col. 4, lines 7-11) connected to the output (Vout) of one or more delay stages (three stages), wherein the switched-controlled load circuitry substantially shields the delay stages from noise (this functional limitation is inherently present in the structure because the structure is the same manner as recited in the claim) in a power supply (VDD) connected to the switch-controlled load circuitry (21, 22, 24).

Regarding Claim 2, Figure 9 shows the switch-controlled load circuitry (21, 22, 24) connected the output (Vout) of each delay stage (30).

Regarding Claims 3, 4, Figure 9 shows switch-controlled load circuitry (21, 22, 24) selectively (ON and OFF by transistor 24) (see Col. 3, lines 28-39) applies a load (capacitive load, 22) to the corresponding delay stage output (Vout).

Regarding Claim 5, Figure 9 shows a ring oscillator.

Regarding Claim 6, Figure 9 shows a VCO (see Col.4, lines 29-45) where the gain of each delay stage is a function of an applied control voltage (Vc) (It is inherent that gain of each delay stage is function of charging current which is a function of an applied control voltage Vc). It is also noted that Figure 7a shows variable current source 31 that is to control the gain of each delay stage in addition to Vc (see Col. 3, lines 53-65).

Regarding Claim 7, Figures 4 and 9 show, for each delay stage output, the switch-controlled load circuitry (21, 22, 24), is connected between the power supply (VDD) and the delay stage output (Vout) and comprises a current source (21), a load (capacitor 22) and a switch (24), where the switch is adapted to selectively (ON and OFF by transistor 24) (see Col. 3, lines 28-39) apply the load to the delay stage output (Vout).

Regarding Claim 8, Figures 4 and 9 show the impedance of the current source substantially decouples the load from the power supply (This limitation is inherently present in the structure because the load, capacitor 22 is directly connected to the current source 21 and ground which is substantially the same arrangement in the application circuitry).

Regarding Claim 9, Figure 4 shows a constant current source (fixed current source 21).

Regarding Claim 16, the functional recitation is inherently present in the structure because the PLL shown in Figure 10 intrinsically provides a specific threshold frequency

in order to lock the desire frequency. In process of locking, each switch (transistor 24) is closed or open based on the control voltage Vc (See Col.3, lines 1-39).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tran in view of Vikinski.

As noted above Tran discloses a circuit as recited in claim 1. However the capacitive load, Capacitor 22 is not of a transistor.

As would have been well known in the art, a transistor-capacitor is used for simplicity in integration fabrication process; for example, Vikinski shows a typical time delay buffer circuit with a capacitive load 220 in Figure 2.

Therefore, it would have been obvious to one of ordinary skill in the art to use such a transistor as a capacitor because it would have advantageously provided simplicity in integration fabrication process.

Allowable Subject Matter

Claims 18-21 are allowed.

Claims 11-15, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the best prior art of record, Tran, taken alone or in combination of other references, does not teach or fairly suggest a connection arrangement of the transistor (Claims 11-15, 17-21). Regarding Claim 21, the claim limitation is construed as a means plus function language and the corresponding structure disclosed in the specification.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ozawa et al. discloses a delay circuit including a charge pump.

Ooishi discloses a delay circuit having constant delay time.

Hayashi et al. discloses a variable delay circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Chang whose telephone number is 571 272-1759. The examiner can normally be reached on Mon-Fri 0700-1730.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph Chang
Patent Examiner
Art Unit 2817